IN THE SPECIFICATION:

Please amend the paragraph beginning at page 8, line 11 and ending at page 9, line 6, to read as follows:

> As stated above, read/write drive circuitry 12 may provide to data output terminals of memory device 1 data values stored in addressed memory cells 2 during memory read operations, and provide to addressed memory cells 2 data appearing at data input terminals of memory device 1 during memory write operations. Read/write drive circuitry 12 may include read drive circuitry 31 having an input coupled to the output of the above-described differential amplifier circuit, and an output coupled to the data output terminals of memory device 1. Read drive circuitry 31 may be designed so that the input switching threshold voltage thereof is between the two (or more) possible output voltage levels of the differential amplifier circuit. For example, the input switching threshold voltage of read drive circuitry 31 may be between a first voltage level appearing at the differential amplifier output corresponding to a logic high data value being stored in the addressed memory cell 2, and a second voltage level appearing at the output corresponding to a logic low data value stored in the addressed memory cell 2. Read drive circuitry 31 may receive a control signal from control circuit 14 and/or address decode circuitry 10 so that data values are placed upon the data output terminals of memory device 1 at certain times, such as towards the end of a memory read operation. It is understood that read drive circuitry 31 ~~29~~ may have any of a number of different circuit implementations.

Please amend the paragraph beginning at page 10, line 11 and ending at page 11, line 5, to read as follows:

> At this point, a differential amplifier circuit is formed for each column corresponding to an addressed memory cell 2. Each differential amplifier circuit is formed by the memory cell 2 in the addressed row, transistor 21 and reference cell 23, along with first load element 27 and second load element 29. For each differential amplifier circuit, the voltage appearing and its output will be based upon the resistance value of resistive element 8 in the addressed memory cell 2. In the event the resistance value of resistive element 8 had been previously programmed to be greater than the resistance value of resistive element 25 in the corresponding reference cell 23, more current passes through second load

element 29 and reference cell 23, resulting in the voltage at the output of the differential amplifier circuit being at a relatively low ~~high~~ voltage level. Conversely, in the event the resistance value of resistive element 8 had been previously programmed to be less than the resistive value of resistive element 25 of the corresponding reference cell 23, less current passes through second load element 29 and reference cell 23, resulting in the voltage appearing at the output of the differential amplifier circuit being at a relatively high ~~low~~ voltage level. Read drive circuitry 31 receives the output of the differential amplifier circuit and drives a data output terminal of memory device 1 to a logic level corresponding to the output voltage of the differential amplifier circuit.